# Tyler Sheaves

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## Summary

Ph.D. candidate specializing in hardware security, side-channel analysis, and secure reconfigurable computing. Experienced in FPGA and embedded system design, digital design, and experimental hardware security research. Former intern with Intel's Programmable Solutions Group (now Altera).

## Education

**University of California, Santa Cruz** 2025–Present
Ph.D. in Computer Science and Engineering *Defending June 2026*
Advisor: Prof. Dustin Richmond | Transferred from UC Davis

**University of California, Davis** 2020–2025
Ph.D. program in Electrical and Computer Engineering

**San Francisco State University** 2012–2017
B.S. in Electrical Engineering

## Experience

**Graduate Student Researcher**, UC Santa Cruz 2025–Present

- ◇ Discovered novel ReRAM timing side-channel on commercial crossbar memories.
- ◇ Designed SAT-assisted ECC reverse engineering technique using timing measurements.
- ◇ Demonstrated successful recovery of full ECC on two commercial ReRAM products.
- ◇ Evaluated commercial ReRAM as NIST-compliant entropy source.
- ◇ Designed novel ReRAM-based TRNG conditioning and monitoring techniques.

**Graduate Student Researcher**, UC Davis 2020–2024

- ◇ Improved tuning resolution of time-to-digital converter side-channel sensor by 50x.
- ◇ Developed post-synthesis obfuscation techniques, taped out test chip in TSMC 65nm.
- ◇ Modeled novel hardware Trojan threat vectors in commercial IP supply chains.
- ◇ Developed obfuscation IP blocks using emerging memories (STT, ReRAM).

**Graduate Technical Intern**, Intel PSG (Altera) 2020–2023

- ◇ Presented confidential computing infrastructure at the Intel Federal Summit.
- ◇ Implemented control IP blocks for attestation and key exchange.
- ◇ Integrated IPs with Open FPGA Stack on D5005 and N6000 PAC platforms.
- ◇ Developed FPGA GUI application used for academic and corporate trainings.

**Lecturer & Teaching Assistant**, UCSC / UCD / SFSU 2017–2025

- ◇ TA for Digital I/II, Computer Architecture, Embedded Systems, and HW Security.
- ◇ Lecturer for Intro to MCUs and Digital Design Verification at SF State.

## Technical Skills

**HW Platforms:** FPGA/SoC-FPGA (Altera), Embedded ARM & RISC-V, PAC D5005 & N6000.
**Languages:** Verilog & System Verilog for RTL & verification, Python, C/C++, Tcl/Tk.
**Tools:** Quartus/ModelSim, Cocotb, Yocto, SAT/SMT solvers, Synopsys digital IC suite, HSPICE.

## Leadership & Service

**Volunteer**, Non-volatile Memories Workshop (NVMW) 2026
**Session Moderator**, Workshop on Open-Source EDA Technology (WOSET) 2024
**Co-chair, Tutorials & Workshops**, International Symposium on FPGAs (ISFPGA) 2023

## Publications

- **T. Sheaves**, A. Althoff, and D. Richmond, "BREW-RC: Bit-exact recovery of ECCs from write timing in ReRAM crossbars," in *2026 63rd ACM/IEEE Design Automation Conference (DAC)*, Accepted, IEEE, 2026.
- C. Drewes, **T. Sheaves**, O. Weng, K. Ryan, B. Hunter, C. McCarty, R. Kastner, and D. Richmond, "Turn on, tune in, listen up: Maximizing side-channel recovery in cross-platform time-to-digital converters," *ACM Transactions on Reconfigurable Technology and Systems*, 2024, Co-first author. DOI: 10.1145/3666092.
- A. Zeraatkar, P. Kamran, I. Kaur, N. Ramu, **T. Sheaves**, and H. Al-Asaad, "On the performance of malware detection classifiers using hardware performance counters," in *2024 International Conference on Smart Applications, Communications and Networking (SmartNets)*, IEEE, 2024, pp. 1–6. DOI: 10.1109/SmartNets61466.2024.10577644.
- C. Fang, N. Miao, H. Wang, J. Zhou, **T. Sheaves**, J. M. Emmert, A. Sasan, and H. Homayoun, "Gotcha! i know what you are doing on the fpga cloud: Fingerprinting co-located cloud fpga accelerators via measuring communication links," in *Proceedings of the ACM SIGSAC Conference on Computer and Communications Security*, 2023, pp. 2024–2037. DOI: 10.1145/3576915.3616606.
- K. I. Gubbi, B. S. Latibari, A. Srikanth, **T. Sheaves**, S. A. Beheshti-Shirazi, S. M. Pd, S. Rafatirad, A. Sasan, H. Homayoun, and S. Salehi, "Hardware trojan detection using machine learning: A tutorial," *ACM Transactions on Embedded Computing Systems*, 2023. DOI: 10.1145/3579823.
- K. I. Gubbi, S. A. Beheshti-Shirazi, **T. Sheaves**, S. Salehi, P. D. S. Manoj, S. Rafatirad, A. Sasan, and H. Homayoun, "Survey of machine learning for electronic design automation," in *Great Lakes Symposium on VLSI*, 2022. DOI: 10.1145/3526241.3530834.
- G. Kolhe, **T. Sheaves**, D. S. M. P., H. Mahmoodi, S. Rafatirad, A. Sasan, and H. Homayoun, "Breaking the design and security trade-off of look-up-table–based obfuscation," *ACM Transactions on Design Automation of Electronic Systems*, vol. 27, 2022. DOI: 10.1145/3510421.
- G. Kolhe, **T. Sheaves**, K. I. Gubbi, S. Salehi, S. Rafatirad, P. D. S. Manoj, A. Sasan, and H. Homayoun, "Lock&roll: Deep-learning power side-channel attack mitigation using emerging reconfigurable devices and logic locking," in *59th ACM/IEEE Design Automation Conference*, 2022. DOI: 10.1145/3489517.3530414.
- S. Salehi, **T. Sheaves**, K. I. Gubbi, S. A. Beheshti, D. S. M. P., S. Rafatirad, A. Sasan, T. Mohsenin, and H. Homayoun, "Neuromorphic-enabled security for iot," in *20th IEEE Interregional NEWCAS Conference*, 2022. DOI: 10.1109/NEWCAS52662.2022.9842256.
- G. Kolhe, S. Salehi, **T. D. Sheaves**, H. Homayoun, S. Rafatirad, M. P. D. Sai, and A. Sasan, "Securing hardware via dynamic obfuscation utilizing reconfigurable interconnect and logic blocks," in *58th ACM/IEEE Design Automation Conference*, 2021. DOI: 10.1109/DAC18074.2021.9586242.
- G. Kolhe, H. M. Kamali, M. Naicker, **T. D. Sheaves**, H. Mahmoodi, P. S. Manoj, H. Homayoun, S. Rafatirad, and A. Sasan, "Security and complexity analysis of lut-based obfuscation: From blueprint to reality," in *IEEE/ACM International Conference on Computer-Aided Design*, 2019. DOI: 10.1109/ICCAD45719.2019.8942100.
- A. Attaran, **T. Sheaves**, P. Mugula, and H. Mahmoodi, "Static design of spin transfer torques magnetic look up tables for asic designs," in *Proceedings of the 2018 Great Lakes Symposium on VLSI*, 2018, pp. 507–510. DOI: 10.1145/3194554.3194651.